Direct Digital Synthesis Primer

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ANALOG DEVICES

Contents

Introduction to DDS

Definition of DDS:

- A ***digital*** technique for generating a sine wave from a fixed-frequency clock source.

Introduction to DDS

DDS "advantages":

- The sine wave FREQUENCY is digitally tunable (typically with sub-Hertz resolution).
- The sine wave PHASE is digitally adjustable, as well, with only a slight increase in circuit complexity.
- Since DDS is digital and the frequency & phase are determined numerically, there are NO ERRORS from drift due to *temperature* or *aging* of components.

Introduction to DDS

DDS “restrictions”:

- The output FREQUENCY must be less than or equal to 1/2 the clock source frequency.
- The sine wave AMPLITUDE is fixed. This can be modified by additional circuitry.
- Since the sine wave is digitally generated by using sampling techniques, the user must be willing to accept a certain amount of DISTORTION. That is, the sine wave is not spectrally “pure”.

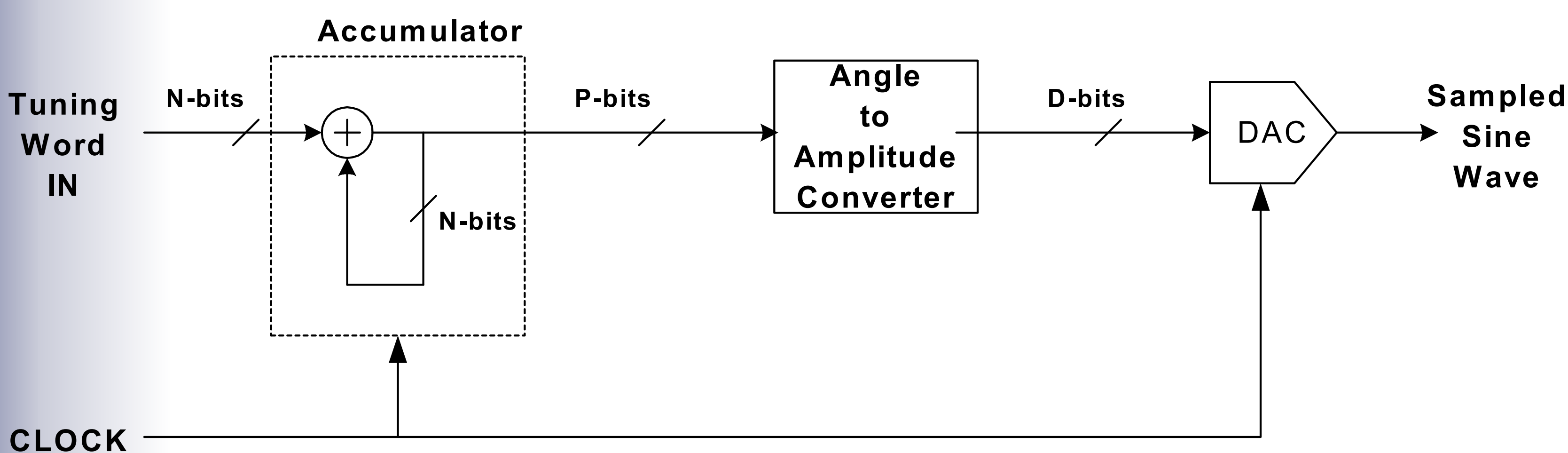
Fundamental DDS Architecture

Basic DDS building blocks:

- **Accumulator**
  - a digital block consisting of an *adder* with feedback
- **Phase-to-Amplitude converter**
  - a digital block that converts digital *phase* values to digital *amplitude* values
- **DAC (Digital-to-Analog Converter)**
  - a digital/analog hybrid that converts digital "numbers" to a scaled analog quantity (voltage or current)
  - Converts the sampled sine wave generated by the digital blocks to a continuous (analog) signal.

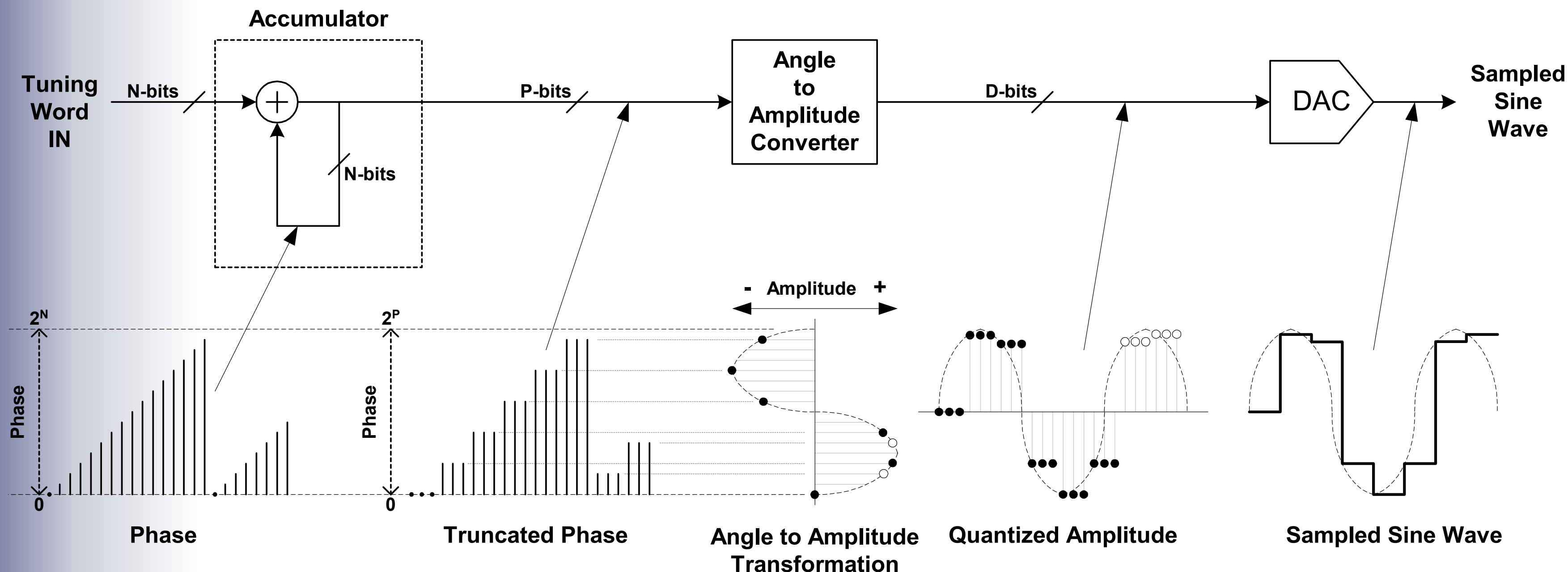
Fundamental DDS Architecture

A Basic DDS



Fundamental DDS Architecture

Sine Wave Synthesis

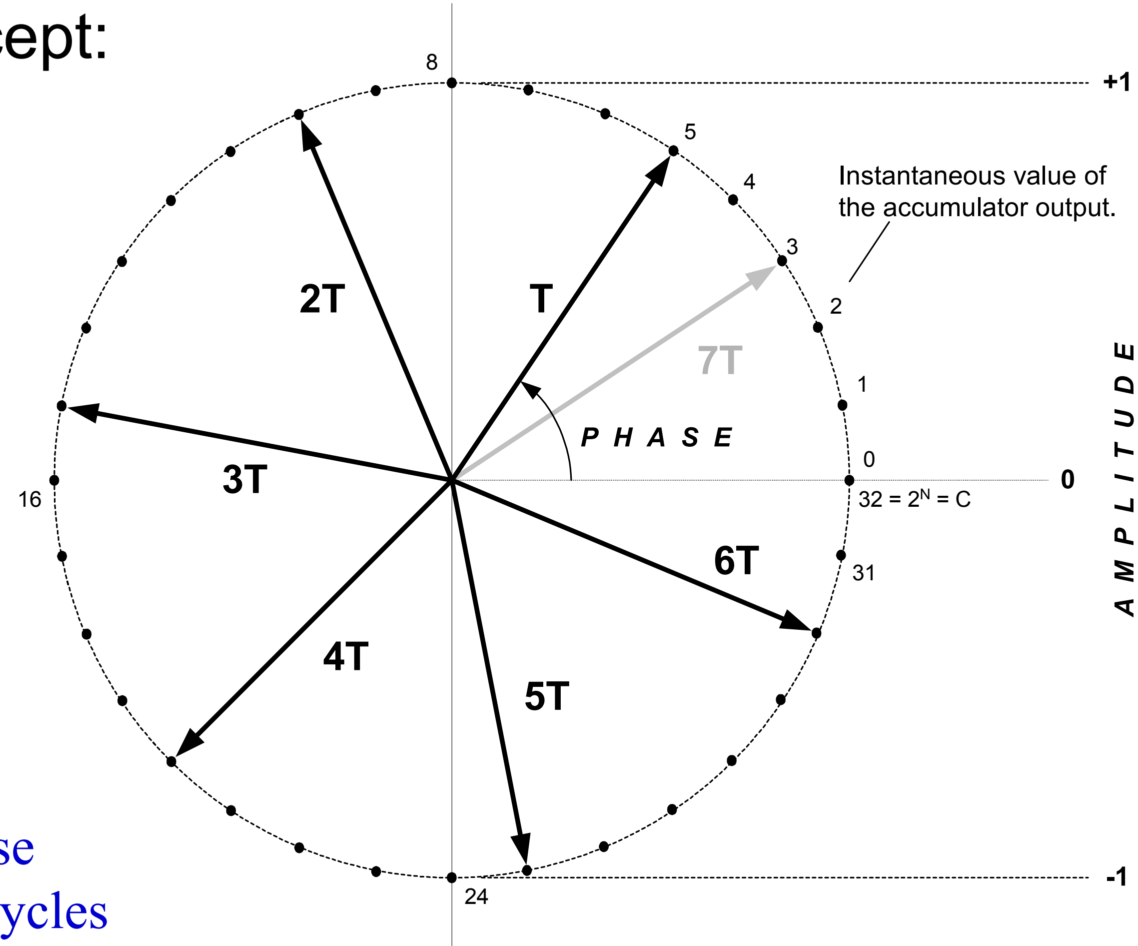


Fundamental DDS Architecture

The "Phase Wheel" Concept:

- **C = 32**
  - •Accumulator capacity
- **T = 5**
  - •Tuning word value
- **N = 6**
  - •Accumulator bits

For this particular case, one revolution around the phase wheel requires 6.4 clock cycles (C/T=6.4).



Fundamental DDS Architecture

Determining the ***output frequency*** (F_o) of a DDS

- F_o depends on 3 parameters:
  - F_s -- the DDS *clock* frequency
  - C -- the accumulator *capacity*
    - where $C = 2^N$
  - T -- the tuning word value
    - where $0 < T < C/2$
- Definition of frequency:
- $f = \delta\Phi/\delta t$ (i.e., the derivative of *phase* w.r.t. *time)*

Fundamental DDS Architecture

DDS output frequency (cont'd)

- δt is the duration of a DDS time step, namely $1/F_s$.
  - $\delta t = 1/F_s$
- $\delta\Phi$ is the phase angle change in time interval, δt.
  - Note that the tuning word is the amount by which the accumulator increments on each DDS time step (δt).
  - Therefore, $\delta\Phi$ is the ratio of the tuning word to the capacity of the accumulator (T/C).
  - Since $C=2^N$, we have:
  - $\delta\Phi = T/2^N$

Fundamental DDS Architecture

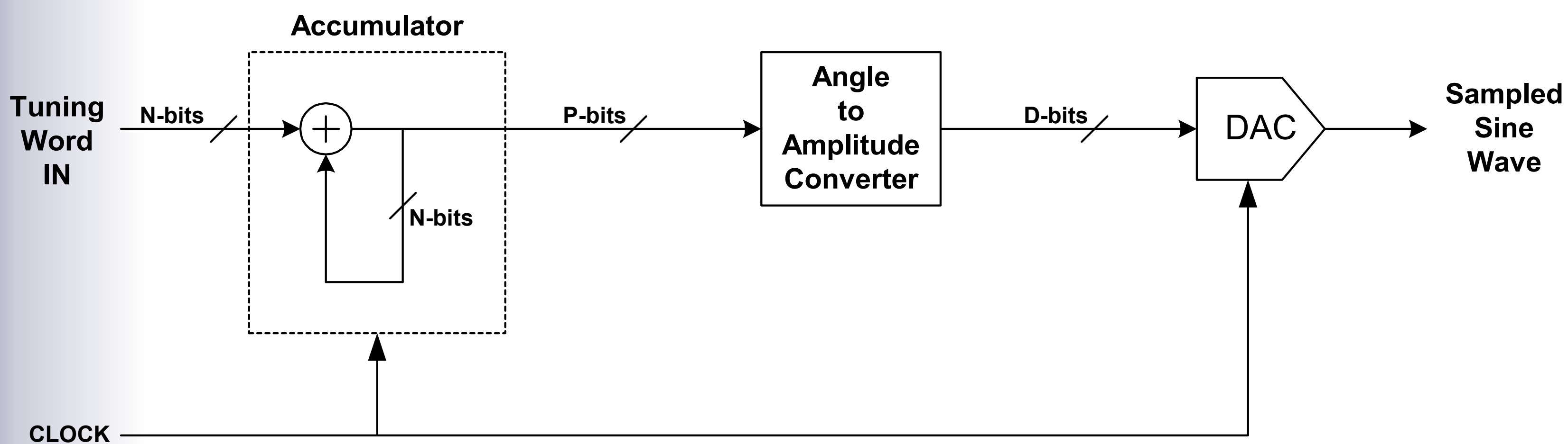
DDS output frequency (cont'd)

- Combining these results gives the <u>frequency</u> (F_o) of the output sine wave as:

$$F_o = F_s T / 2^N$$

Fundamental DDS Architecture

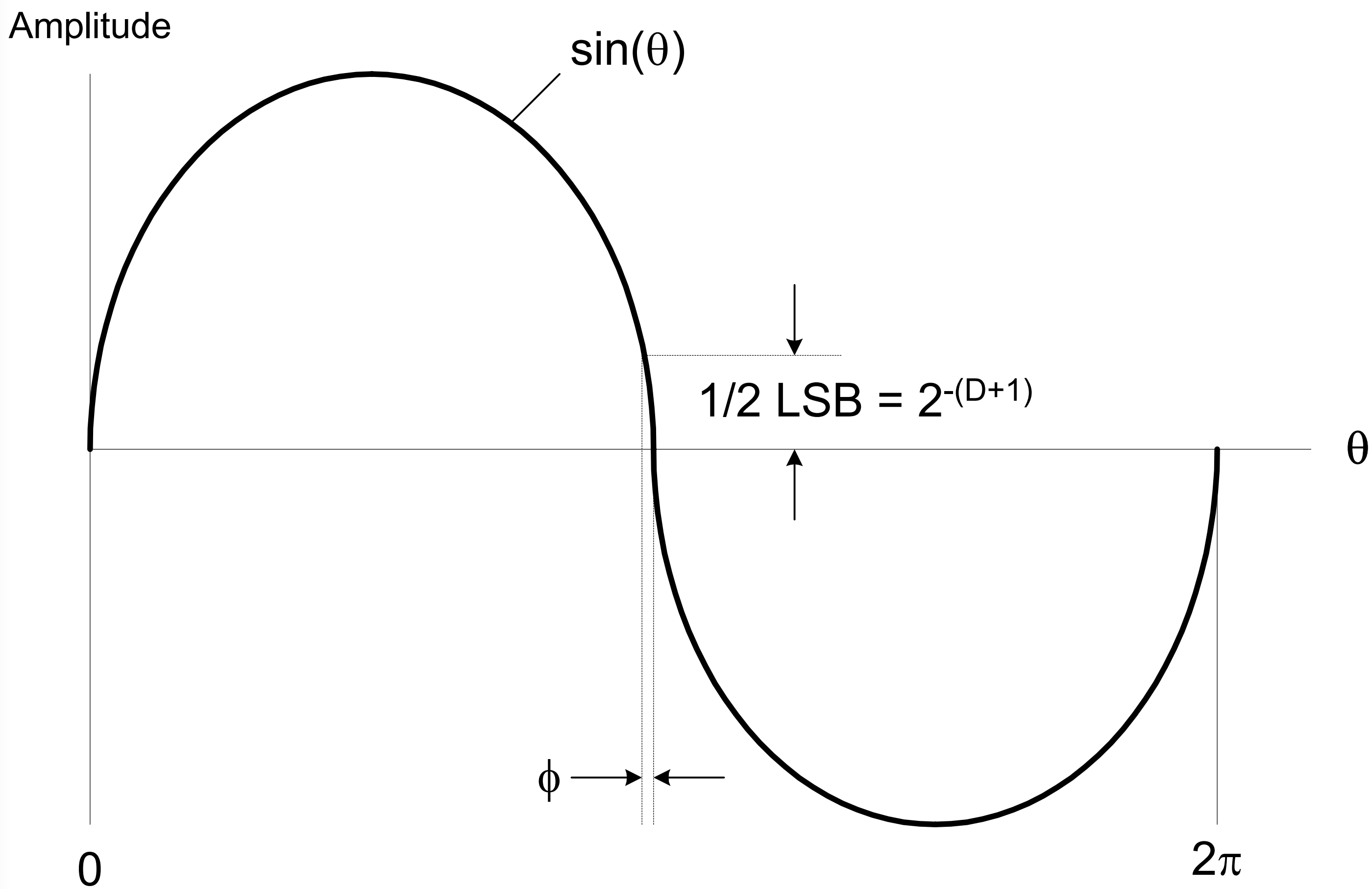
How Many Phase Bits?



The AAC must generate amplitude values that are accurate to 1/2 LSB of the DAC. To accomplish this,

P requires at least 4 more bits than the DAC

Fundamental DDS Architecture

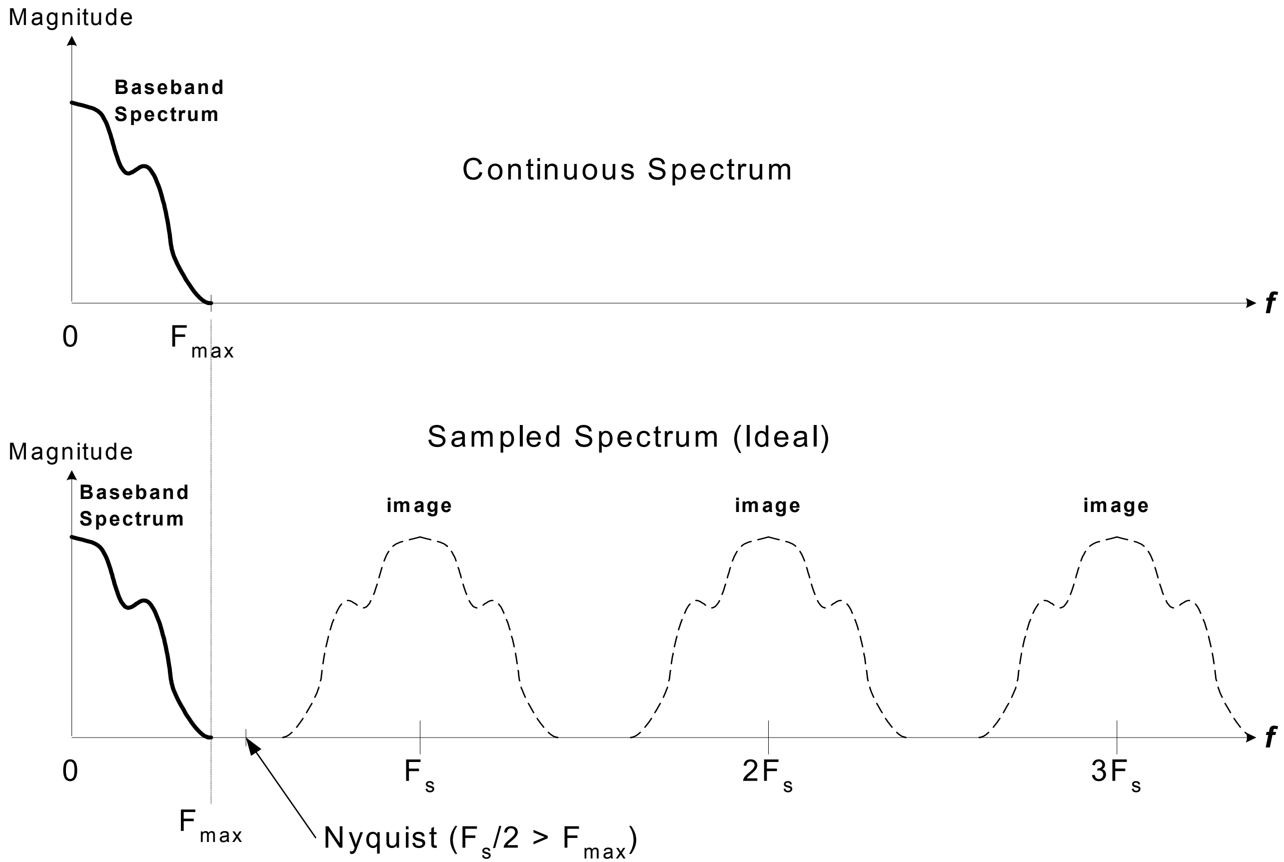


Spectral Characteristics

- DDS is a "sampled data system"
- Sampled nature of DAC output produces replicated spectra ("images") of the output frequency.
- Zero-order-hold characteristic of the DAC causes the spectrum to be attenuated according to the SIN(x)/x (or SINC) envelope.

Spectral Characteristics

Spectral Consequences of Sampling



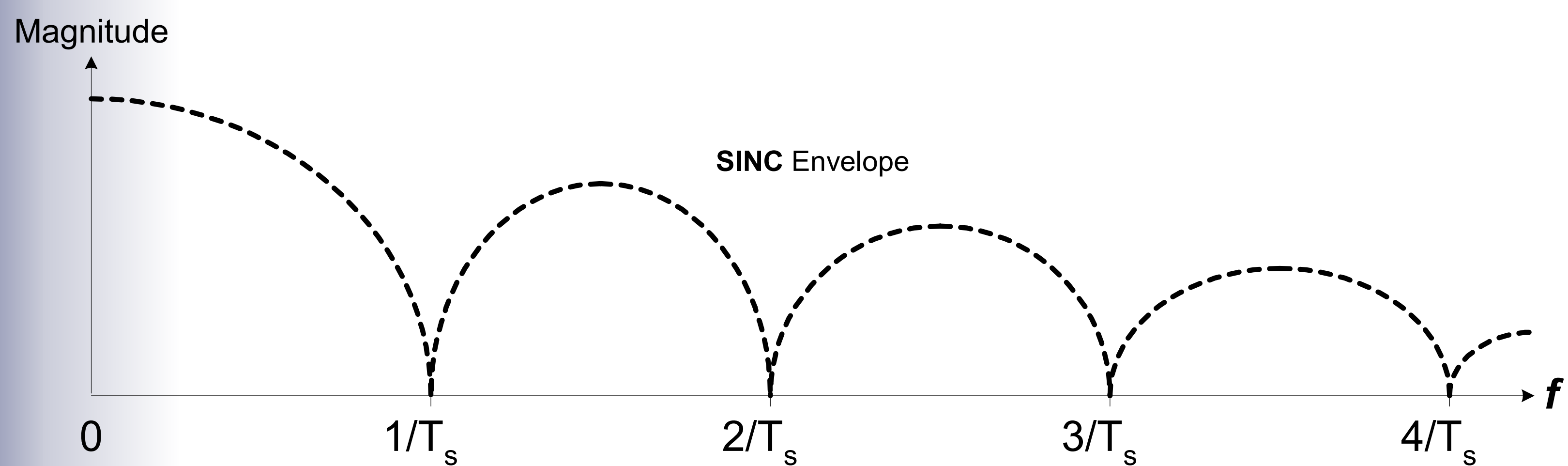
Spectral Characteristics

- "Ideal" sampled spectrum occurs when the sample pulses are infinitely narrow.
  - That is, in the time domain the width of the sample pulses (T_s) approaches 0.
- If the sample pulses have finite width ($T_s > 0$), then SIN(x)/x (or SINC) distortion occurs.
- In the frequency domain, the SINC "envelope" is characterized by lobes with null points at frequencies that are multiples of $1/T_s$.

Spectral Characteristics

SINC Envelope

sin(x)/x

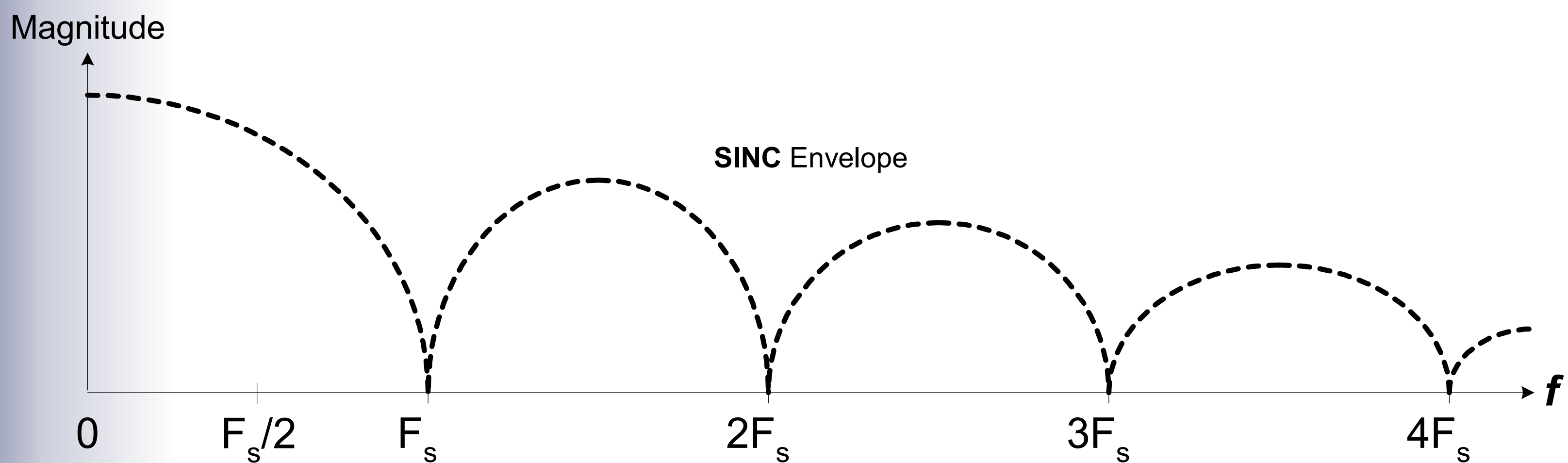


Spectral Characteristics

- In a DDS system, the DAC is clocked at the same rate as the accumulator.
- This is the DDS sample rate, F_s.
- Thus, the minimum width of a sample pulse produced by the DAC is $1/F_s$, which is T_s.
- This means that in a DDS, the nulls of the SINC envelope are coincident with multiples of the DDS sample rate.

Spectral Characteristics

SINC Envelope



Spectral Characteristics

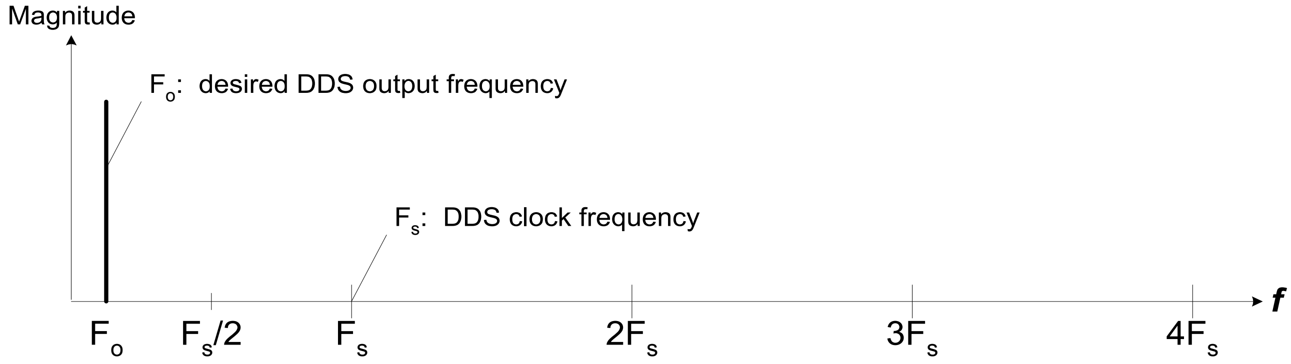
- **SUMMARY**
  - **A DDS is a sampled system**
  - **A sampled system produces images of the baseband spectrum at multiples of the sample rate.**
  - **The finite pulse width resulting from the operation of the DAC distorts the spectrum by attenuating the baseband signal and its images based on the SINC envelope.**

Spectral Characteristics

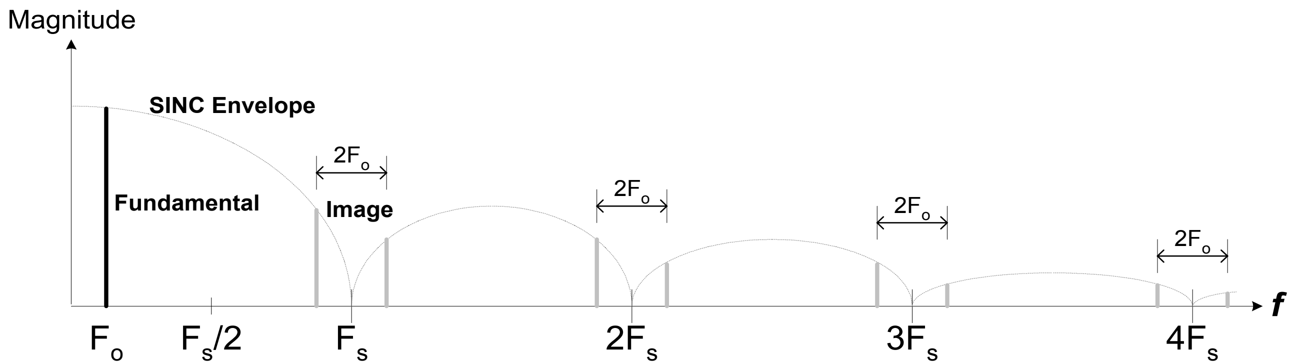
- The output of a basic DDS is a single tone (i.e., a sine wave at a specific frequency).
- Since the DDS is a sampled system, the actual output signal is the desired tone PLUS its images.
- The images must be filtered out in order to provide a spectrally “pure” sine wave.

Spectral Characteristics

Pure vs Synthesized Sine Wave



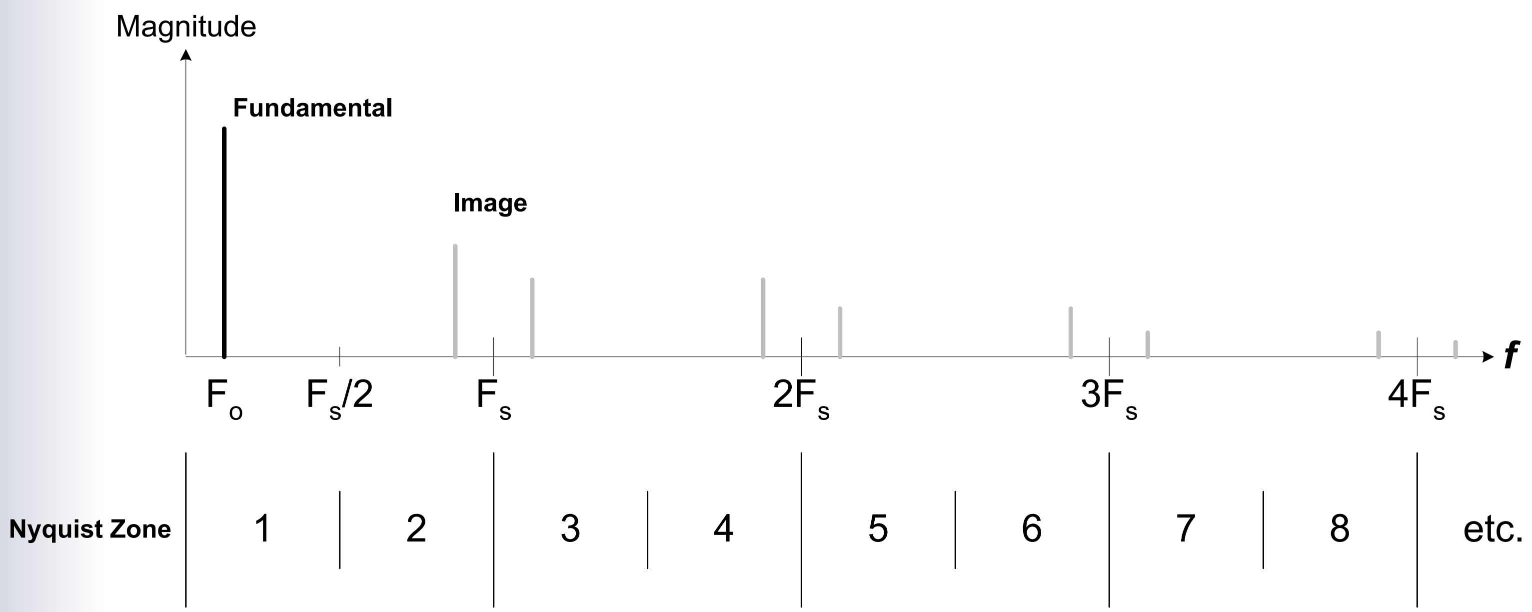
Pure Sine Wave



Sampled Sine Wave

Spectral Characteristics

ODD and EVEN *Nyquist Zones*



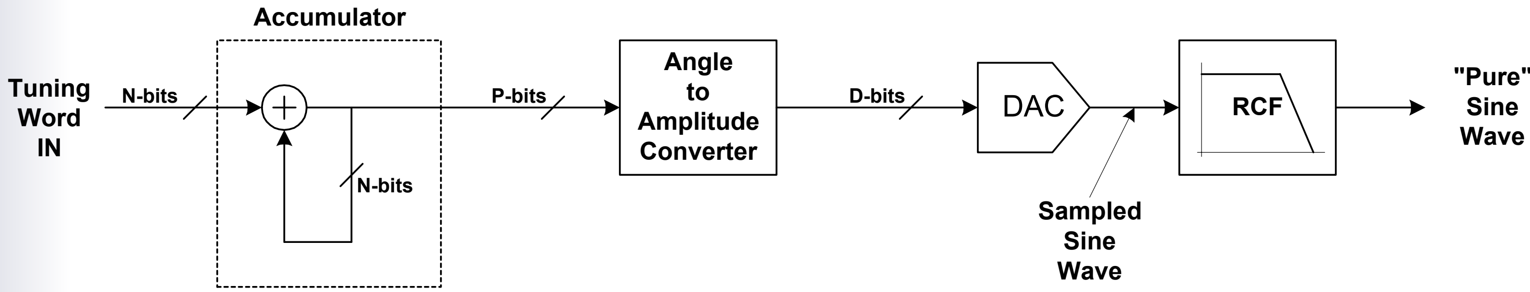
Spectral Characteristics

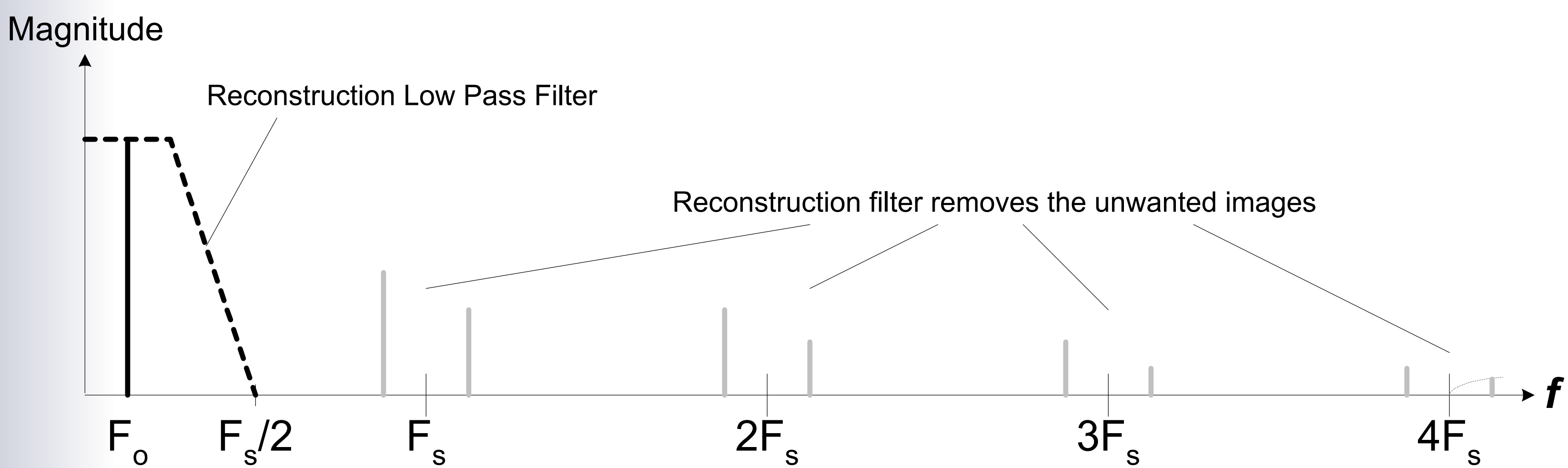
ODD and EVEN *Nyquist Zones*:

- **A Nyquist zone spans a frequency range of $F_s/2$.**
- **ODD zones**
  - **A change in the frequency of the fundamental results in an equal change in frequency of the half image**
- **EVEN zones**
  - **A change in frequency of the fundamental results in an equal *but opposite* (negative) change in the frequency of the half image**

Spectral Characteristics

Filtering the DDS Output





Spectral Characteristics

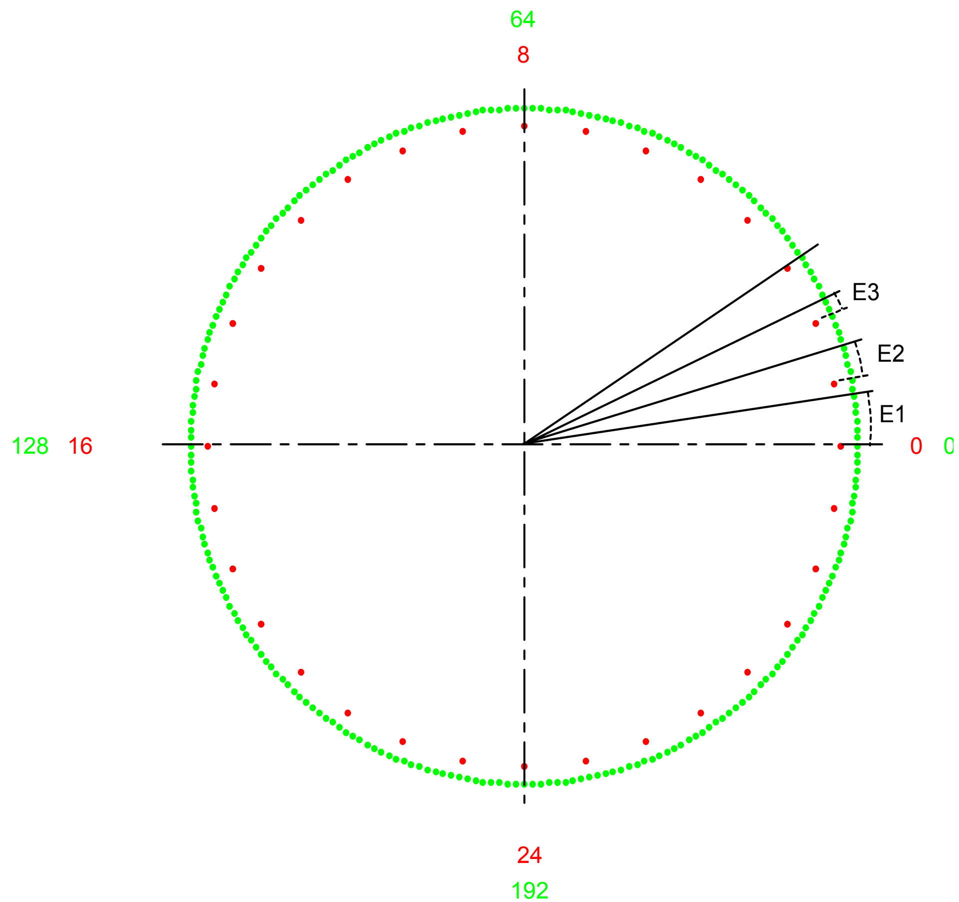
Additional artifacts in the DDS output spectrum:

- **Phase truncation spurs**
- **DAC nonlinearity**
- **DAC switching noise**

Spectral Characteristics
Phase Truncation Spurs

Phase Truncation Error

(8-bit accumulator truncated to 5 bits with a tuning word of 6)



Spectral Characteristics
Phase Truncation Spurs

phase truncation spurs

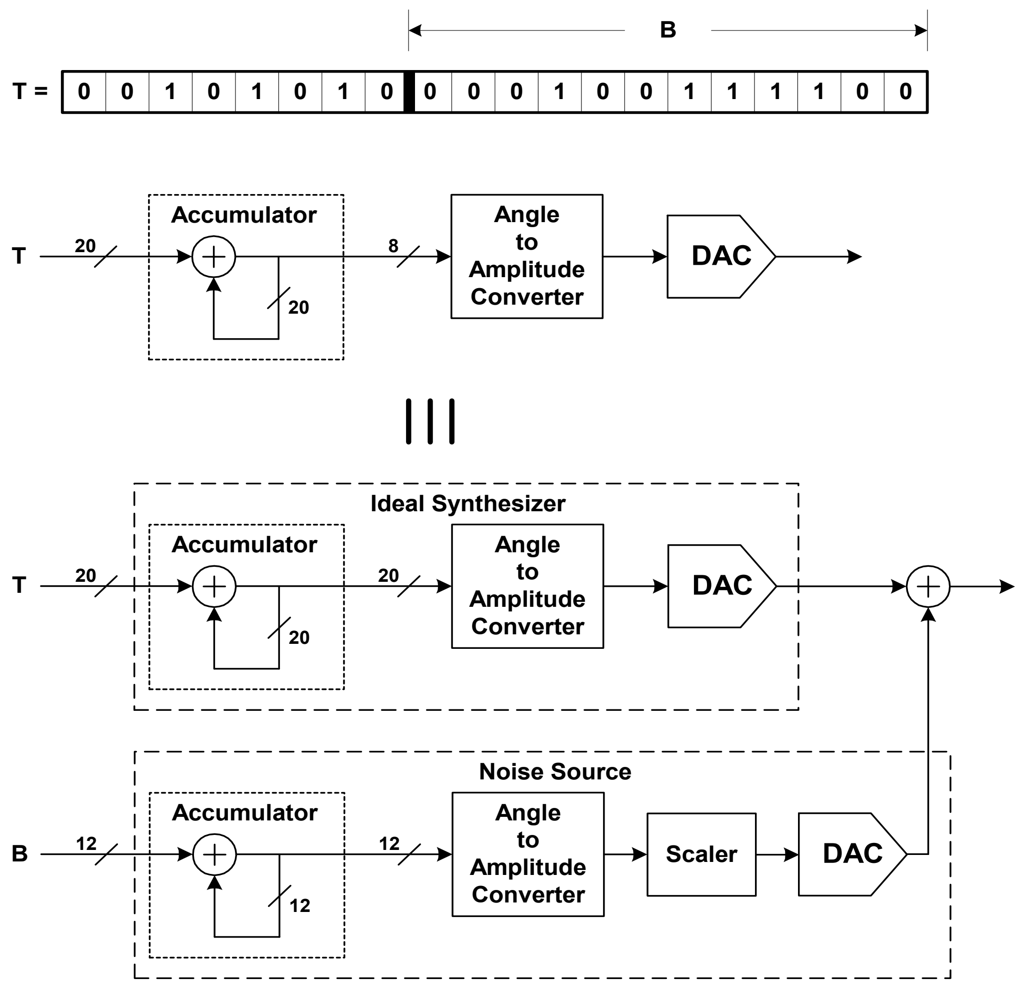
- Rigorous analysis is beyond the scope of this presentation.
- However, a practical explanation follows.

Spectral Characteristics
Phase Truncation Spurs

- The spectral characteristics of phase error are rooted in the time domain behavior of the truncated phase bits.

- The behavior of the truncated phase bits can be thought of as a mini-accumulator of width B with an initial tuning word that is composed of only those bit locations that are truncated.

Spectral Characteristics
Phase Truncation Spurs

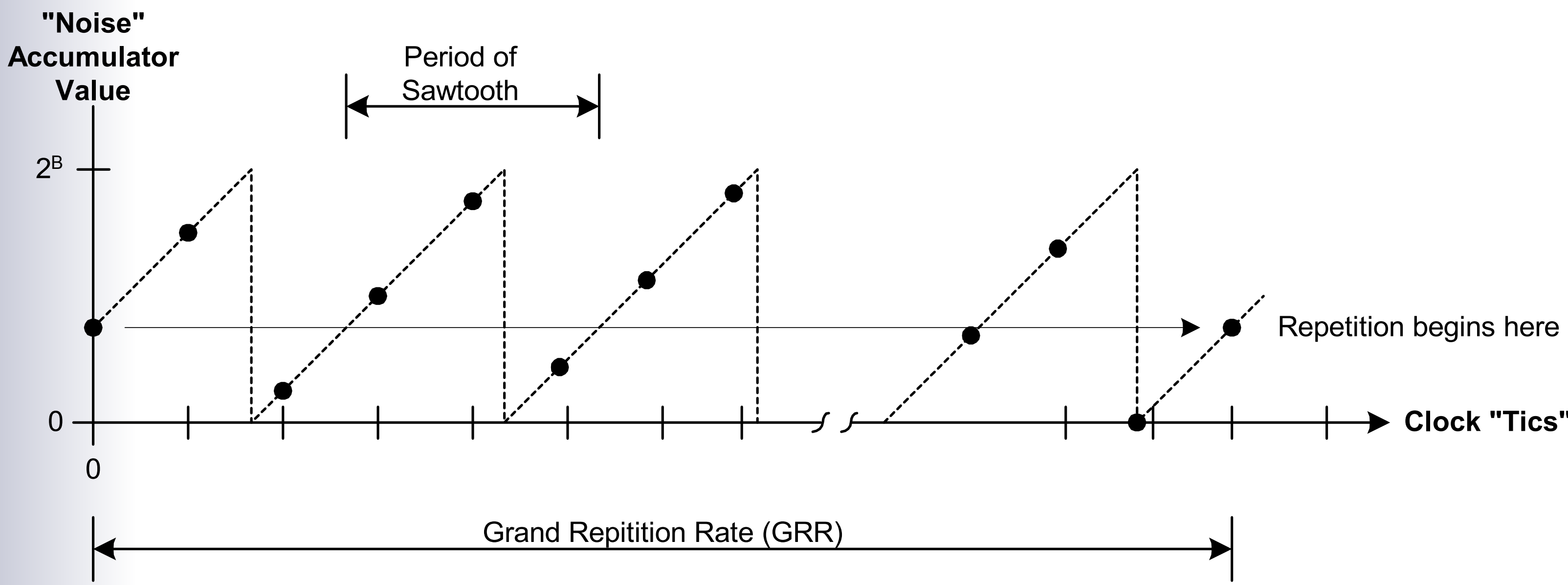


Spectral Characteristics
Phase Truncation Spurs

- The “noise” source is what generates the phase truncation spurs.
- The behavior of the “noise” accumulator is analogous to that of the ideal accumulator, but with its own tuning word.
- The phase error accumulates up to the *CAPACITY* of the noise accumulator. At which point it “rolls over” and the accumulating process resumes.

Spectral Characteristics
Phase Truncation Spurs

Phase Error "Sawtooth" for an Arbitrary Tuning Word

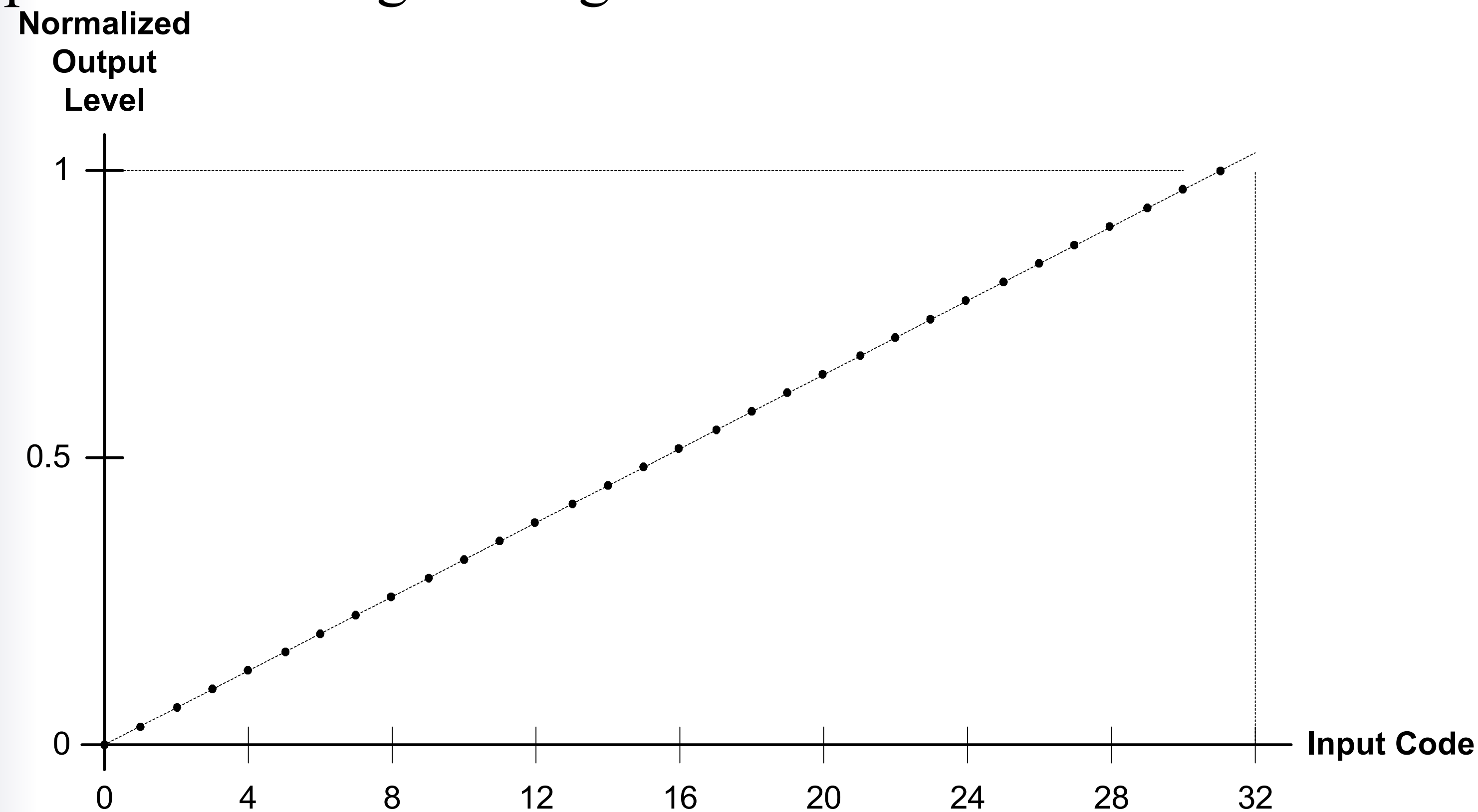


Spectral Characteristics
Phase Truncation Spurs

- Not to worry...
  - A properly designed DDS forces the magnitude of the largest truncation error spur to be less than the 1/2 LSB error of the DAC.
  - Truncation spur energy is comparable to the energy contained in the integrated DAC noise floor.

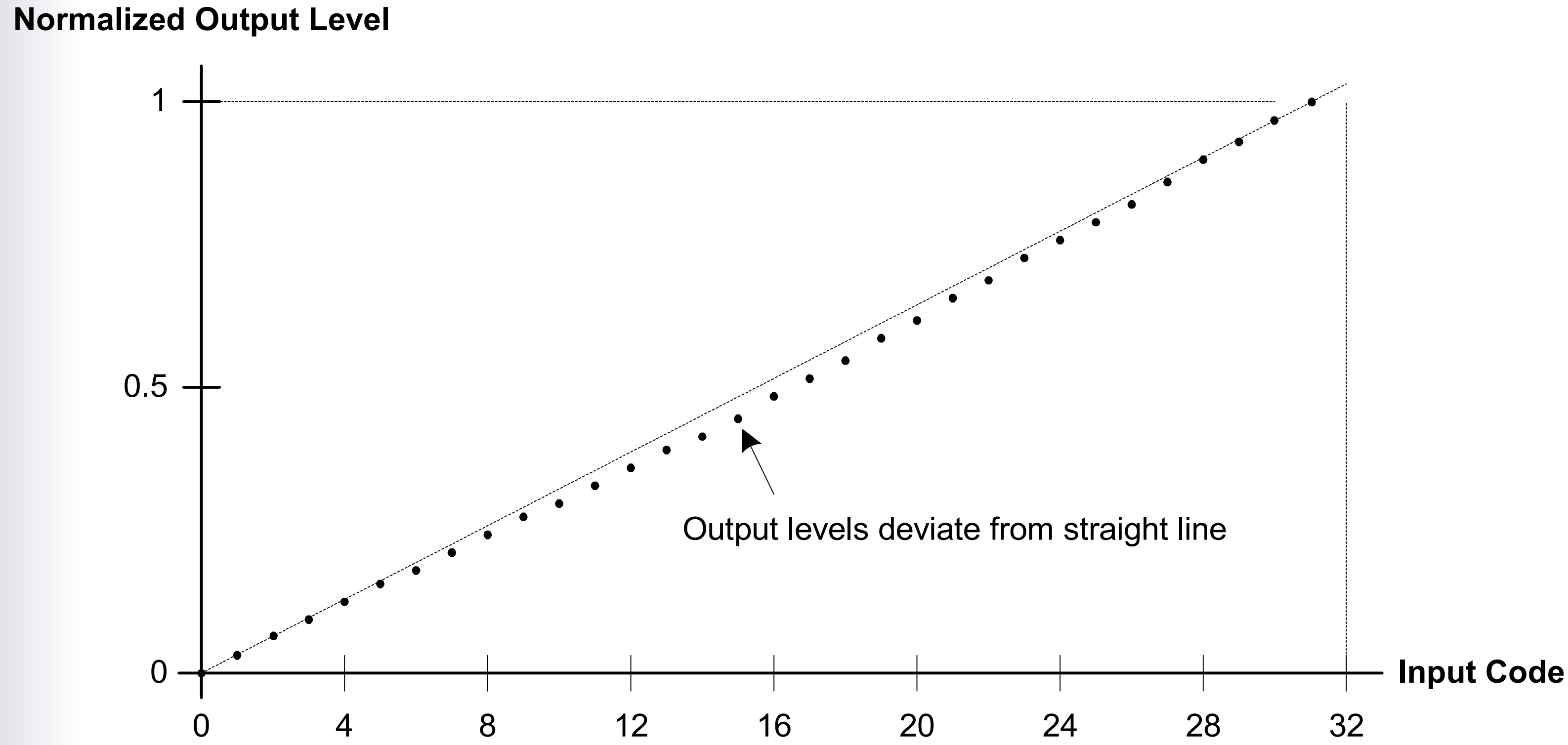
Spectral Characteristics
DAC Nonlinearity

- An "ideal" DAC translates the digital codes at the input to output levels along a straight line.



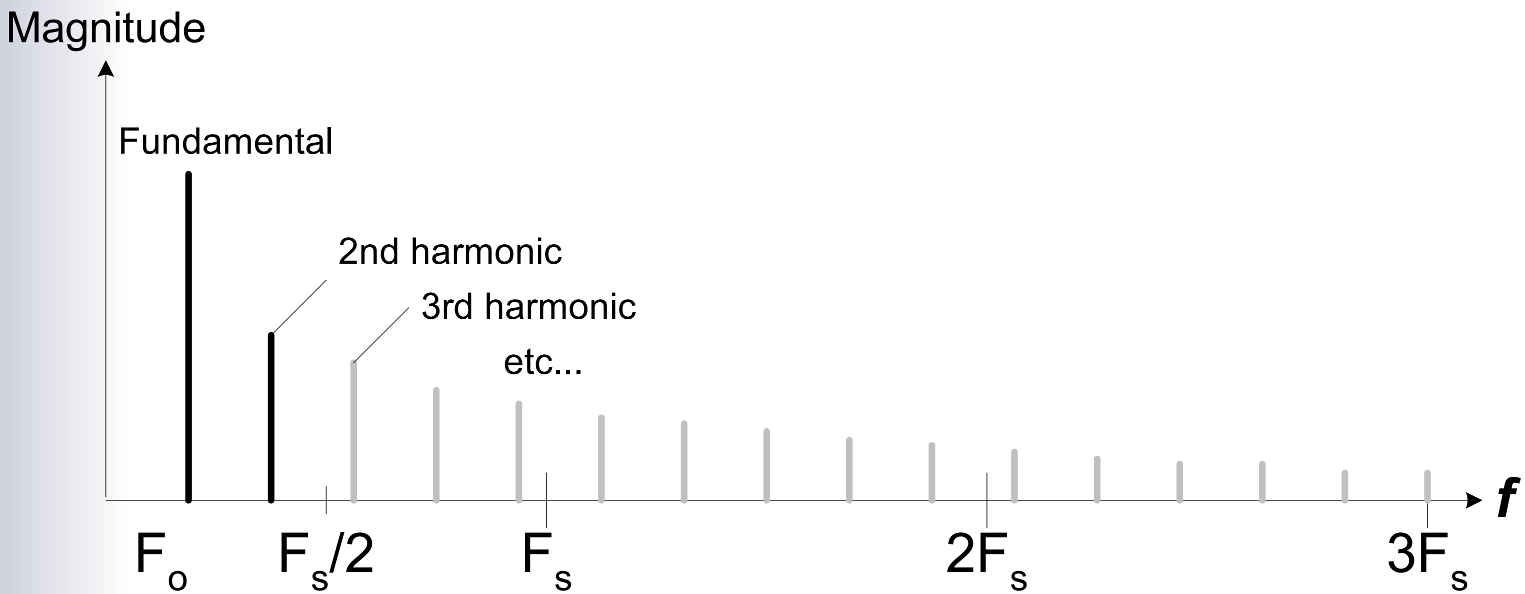
Spectral Characteristics
DAC Nonlinearity

- A "typical" DAC tends to deviate from a straight line.
- This nonlinearity leads to harmonic distortion.



Spectral Characteristics
DAC Nonlinearity

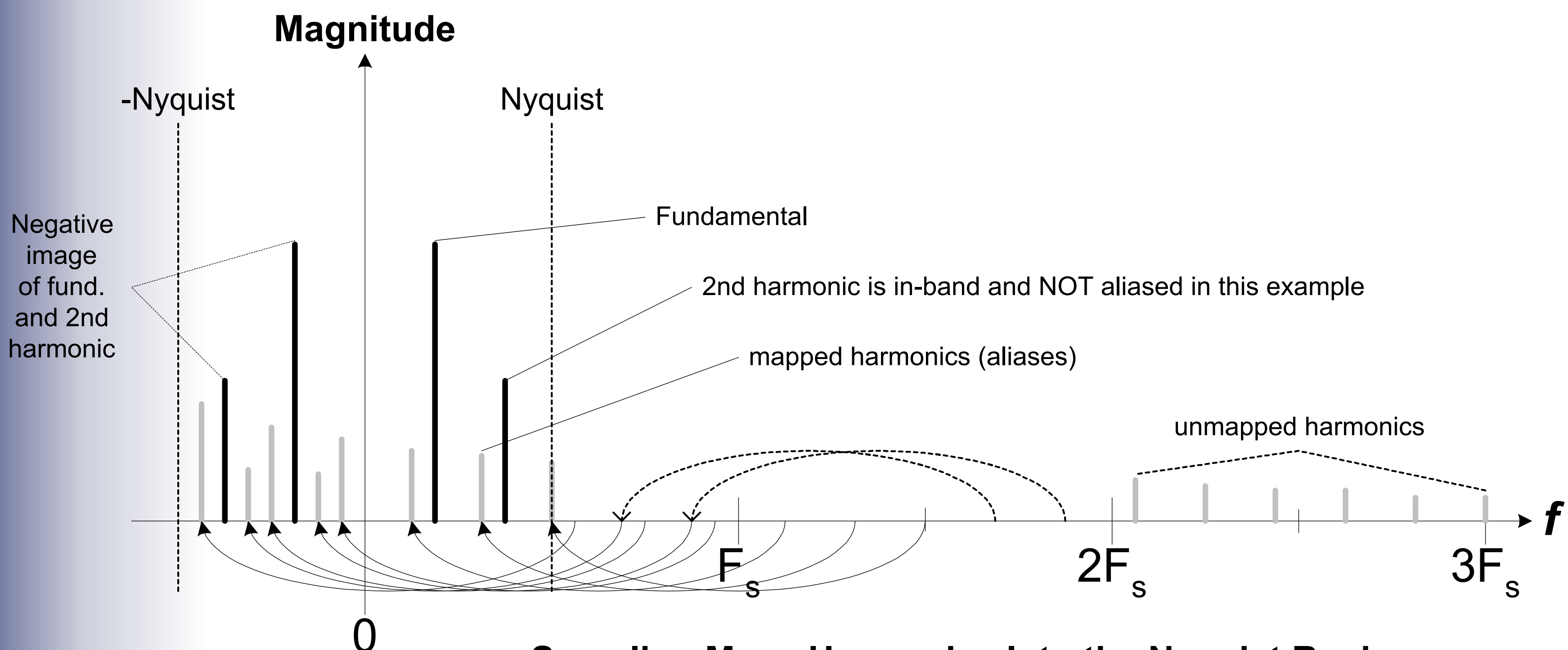
- The nonlinear transfer function produces harmonics of the fundamental which are aliased into the first Nyquist zone.
- First, consider the UNSAMPLED spectrum, below.



Harmonic Distortion (unsampled system)

Spectral Characteristics
DAC Nonlinearity

- Since the DAC is a sampled system, the harmonics must be mapped into the Nyquist region.

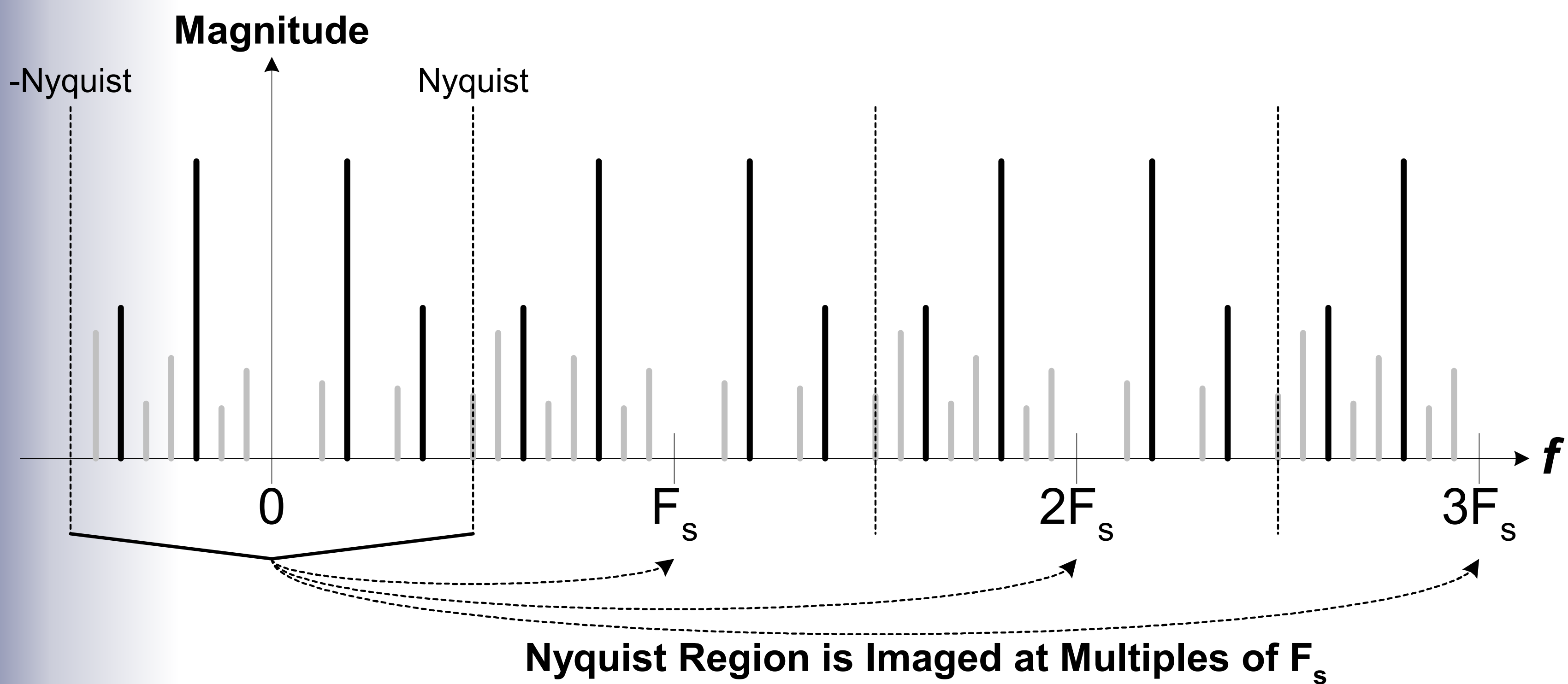


Sampling Maps Harmonics Into the Nyquist Region

Spectral Characteristics
DAC Nonlinearity

- Sampling causes images of the Nyquist region to appear at multiples of F_s.

(Attenuation due to the SINC envelope is not shown)



Spectral Characteristics
DAC Switching Noise

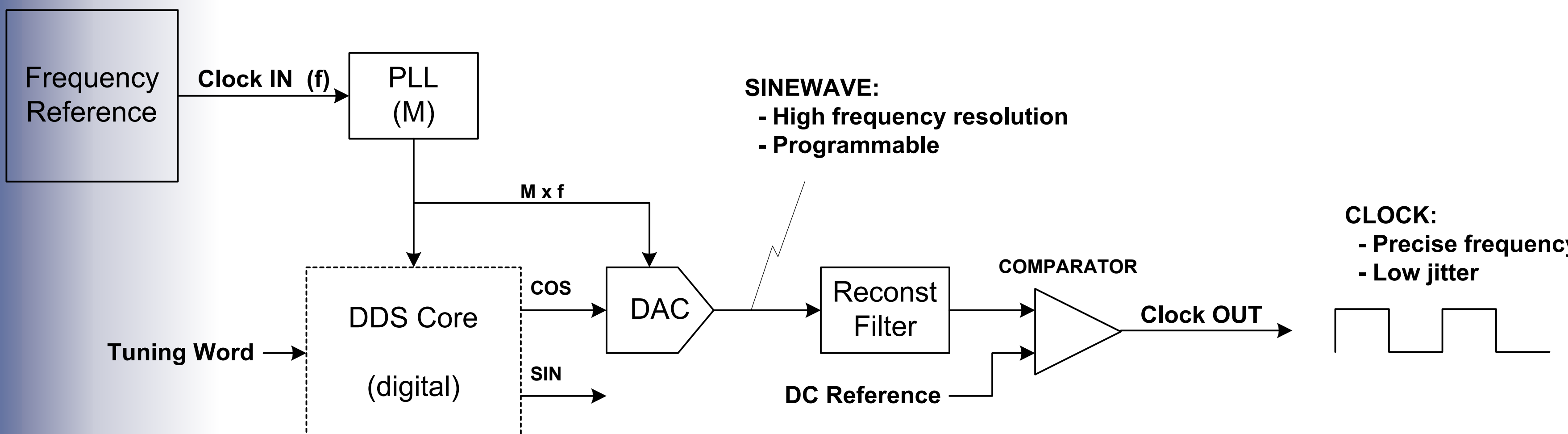
- High slew rate of digital signals internal to the DAC leads to noise transients being coupled to the DAC output pin(s).
- Other high speed signals in close proximity to the DAC from digital circuits on the same silicon die can also couple into the DAC.
- This results in high speed switching transients appearing at the DAC output as a source of noise and further degrades overall performance.

DDS as a Building Block

- The fact that a DDS internally generates a *digital* sinusoidal wave can be used to great advantage.
- Combining the digital DDS core with additional signal processing blocks makes possible:
  - Frequency "agile" clock generators
  - Frequency and/or Phase "agile" modulators
    - FSK, PSK, QPSK, n-QAM, OFDM
  - Frequency swept (chirp) modulators

DDS as a Building Block
Clock Generator

A DDS-based Clock Generator



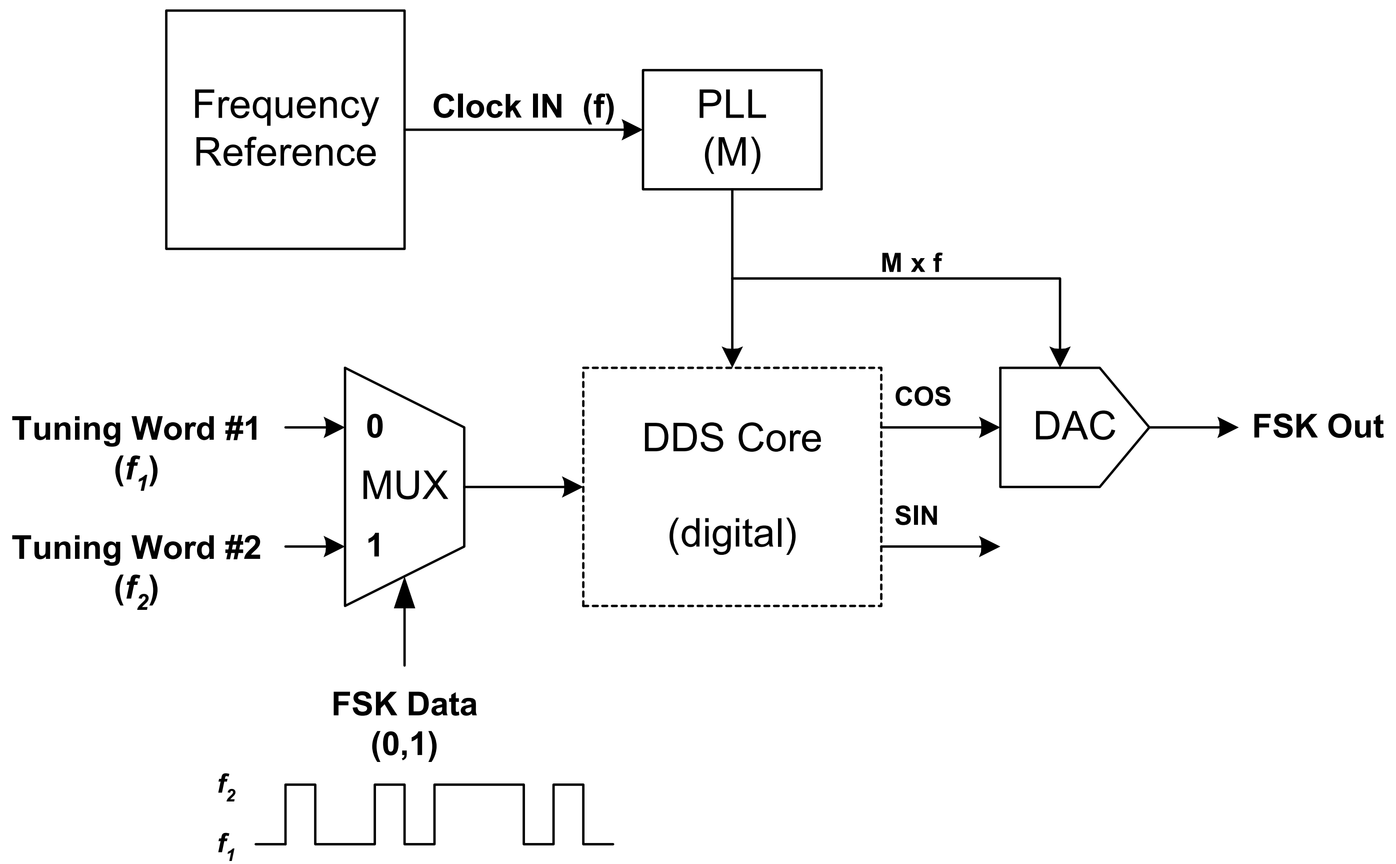
DDS as a Building Block
Digital Modulator

A DDS-based modulator requires some additional digital signal processing blocks:

- Digital multipliers
- Digital adders
- Input logic to accept digital modulation data
- Data rate translator (optional)

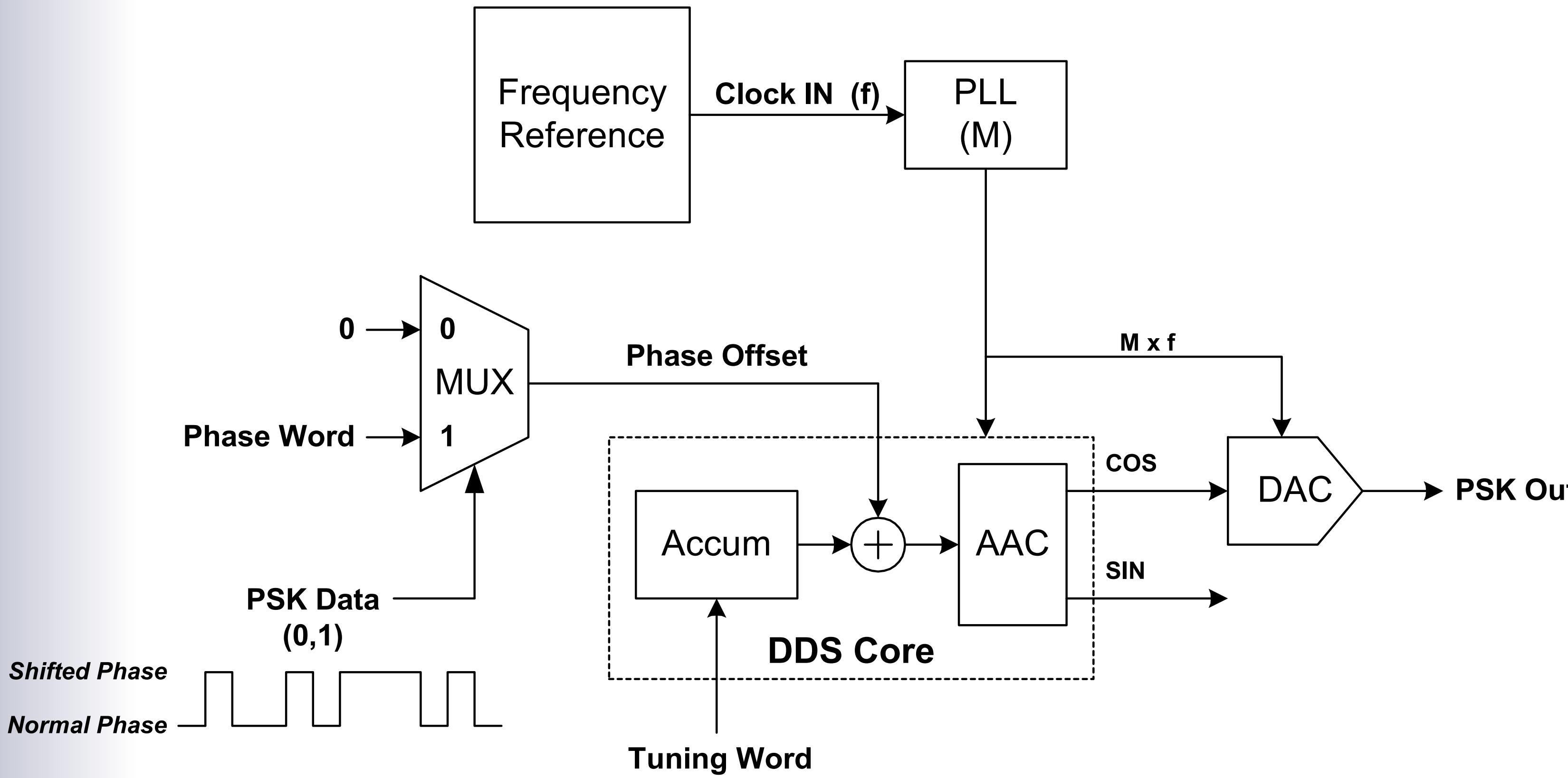
DDS as a Building Block
Digital Modulator

FSK Modulator



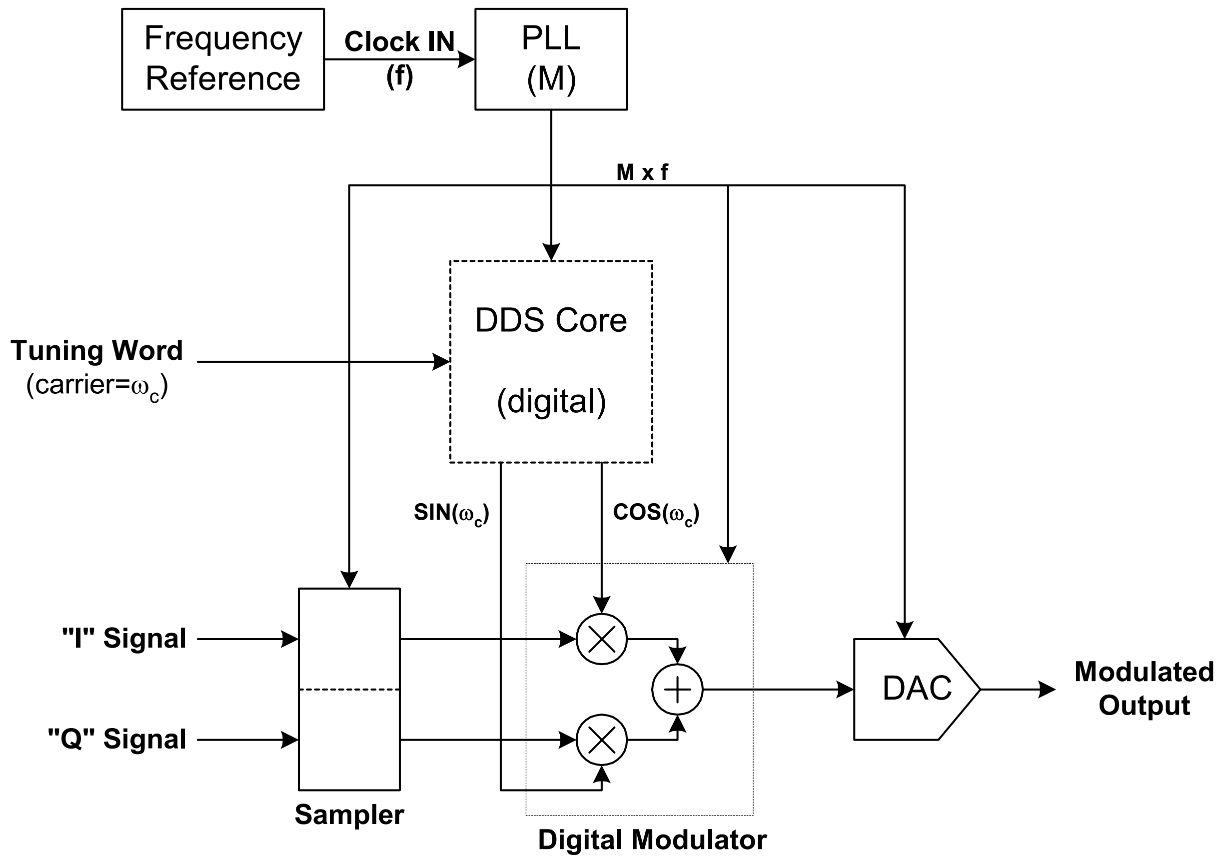
DDS as a Building Block
Digital Modulator

PSK Modulator



DDS as a Building Block
Digital Modulator

Quadrature Modulator



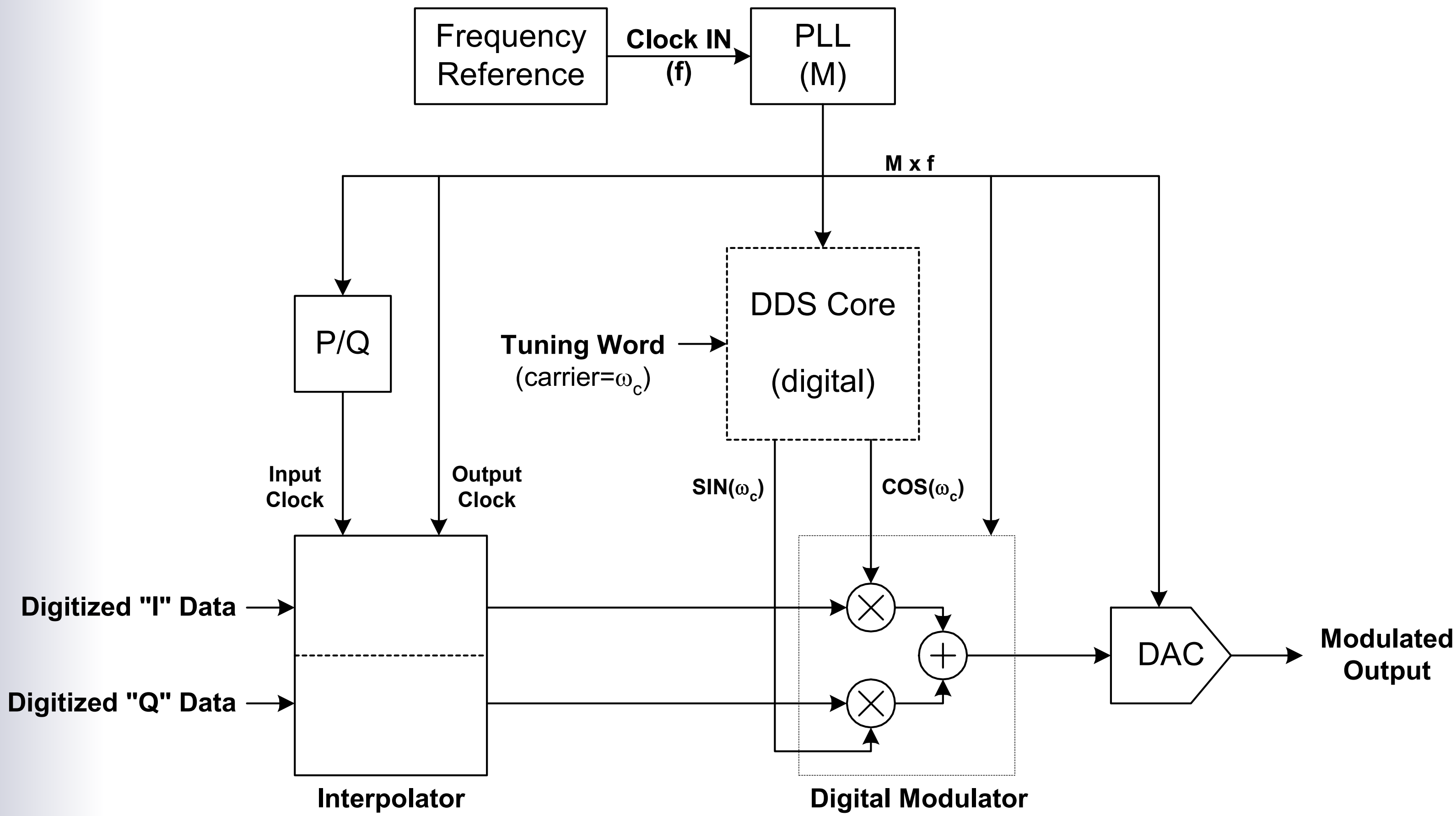
DDS as a Building Block
Quadrature Modulation Rule

The modulation signal (I/Q) must be sampled at the same rate as the DDS clock.

- If the modulation signal is sampled at a rate lower than the DDS clock, then rate up-conversion (*interpolation*) is required to synchronize the sampled modulation data with the sampled carrier (the DDS output).
- Furthermore, the DDS and modulation data sample rates should have, at the very least, a *rational* ratio (i.e., P/Q where P and Q are integers).
  - An integer ratio offers better hardware efficiency than a rational ratio.
  - A power-of-2 ratio is the most hardware efficient of all.

DDS as a Building Block
Digital Modulator

Quadrature Up-Converter



DDS as a Building Block
Chirp Modulator

Chirp Modulator:

- A form of FM (frequency modulation)
- Requires the output signal to start at one frequency and gradually "sweep" to another.
- For a DDS, this means repeatedly changing the tuning word value from a value of T_1 to T_2 with a step size (ΔT) such that the "sweep" time requirement is met.
- *A dual-accumulator* DDS effectively accomplishes the "frequency sweep" function.

DDS as a Building Block
Chirp Modulator